In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A UMOSFET, comprising:

a semiconductor substrate;

a first trench in said substrate;

an insulated gate electrode in said first trench; and

a source electrode in said first trench, extending between said insulated gate electrode and a bottom of said first trench.

2. The UMOSFET of claim **1**, wherein said substrate contains a graded-doped drift region therein.

3. The UMOSFET of claim **1**, further comprising:

a second trench in said substrate, adjacent said first trench;

a first field plate insulating region lining said second trench; and

a field plate on said first field plate insulating region.

4. The UMOSFET of claim **3**, further comprising:

a second field plate insulating region on a face of said substrate; and

a field plate extension on the second field plate insulating region and electrically connected to said field plate.

5. The UMOSFET of claim **4**, wherein said field plate extension and said field plate are electrically connected to said gate electrode or said source electrode.

6. The UMOSFET of claim **1**, further comprising a Schottky rectifying contact on said substrate, adjacent said first trench.

7. A vertical power device, comprising:

a trench in a semiconductor substrate;

a source region of first conductivity type in the semiconductor substrate;

an insulated first source electrode in and adjacent a bottom of said trench;

a second source electrode on the substrate, electrically coupled to said source region and said insulated first source electrode; and

an insulated gate electrode in and adjacent a top of said trench.

8. The device of claim **7**, wherein said trench has first and second opposing sidewalls; and wherein said second source electrode forms an ohmic contact with a portion of said source region extending adjacent the first sidewall and forms a Schottky rectifying contact with a portion of the semiconductor substrate extending adjacent the second sidewall.

9. The device of claim **7**, further comprising:

a base region of second conductivity type in a portion of the semiconductor substrate extending adjacent a first sidewall of said trench; and

a breakdown shielding region of second conductivity type in a portion of the semiconductor substrate extending adjacent a second sidewall of said trench.

10. The device of claim **9**, wherein said breakdown shielding region is more highly doped than said base region.

11. The device of claim **10**, wherein said breakdown shielding region extends deeper into the semiconductor substrate than said base region.

12. The device of claim **9**, wherein said breakdown shielding region extends adjacent the second sidewall of said trench.

13. The device of claim **12**, wherein said breakdown shielding region extends deeper into the semiconductor substrate than said base region.

14. A field effect transistor, comprising:

a semiconductor substrate having first and second opposing faces;

a source region of first conductivity type in said substrate, adjacent the first face;

a drain region of first conductivity type in said substrate, adjacent the second face;

a drift region of first conductivity type in said substrate, said drift region forming a non-rectifying junction with said drain region;

a base region of second conductivity type in said substrate, said base region extending between said source region and said drift region and forming first and second P-N junctions therewith, respectively;

a first trench in said substrate at the first face, said first trench having a sidewall extending adjacent said drift region and said base region and a bottom extending adjacent said drain region;

a gate electrode in said first trench, extending opposite said base region;

a first source electrode in said first trench, said first source electrode extending between said gate electrode and the bottom of said first trench; and

an electrically insulating region in said first trench, said electrically insulating region extending along the sidewall of said first trench and between said gate electrode and said first source electrode.

15. The transistor of claim **14**, wherein said drift region has a graded first conductivity type doping concentration therein which decreases in a direction from said drain region to said base region.

16. The transistor of claim **15**, wherein said electrically insulating region includes a gate insulating region having a first thickness as measured between said gate electrode and the sidewall of said first trench, and a source insulating region having a second thickness as measured between said first source electrode and the sidewall of said first trench; and wherein the second thickness is greater than the first thickness.

17. The transistor of claim **16**, wherein the first thickness is less than about 750 Å; and wherein the second thickness is greater than about 1500 Å.

18. The transistor of claim **16**, further comprising:

a second trench in said substrate at the first face, adjacent said first trench;

a first field plate insulating region having a uniform thickness lining said second trench; and

a field plate in said second trench, on said first field plate insulating region.

19. The transistor of claim **18**, further comprising:

a second field plate insulating region on the first face; and

a field plate extension on the second field plate insulating region, opposite the first face.

20. The transistor of claim **19**, wherein said field plate extension and said field plate are electrically connected together and are electrically connected to said gate electrode or said first source electrode.

21. The transistor of claim **18**, wherein said first and second trenches define a transition mesa region therebetween; and wherein said transition mesa region comprises a breakdown shielding region of second conductivity type therein which forms a third P-N junction with said drift region.